Fig. 1

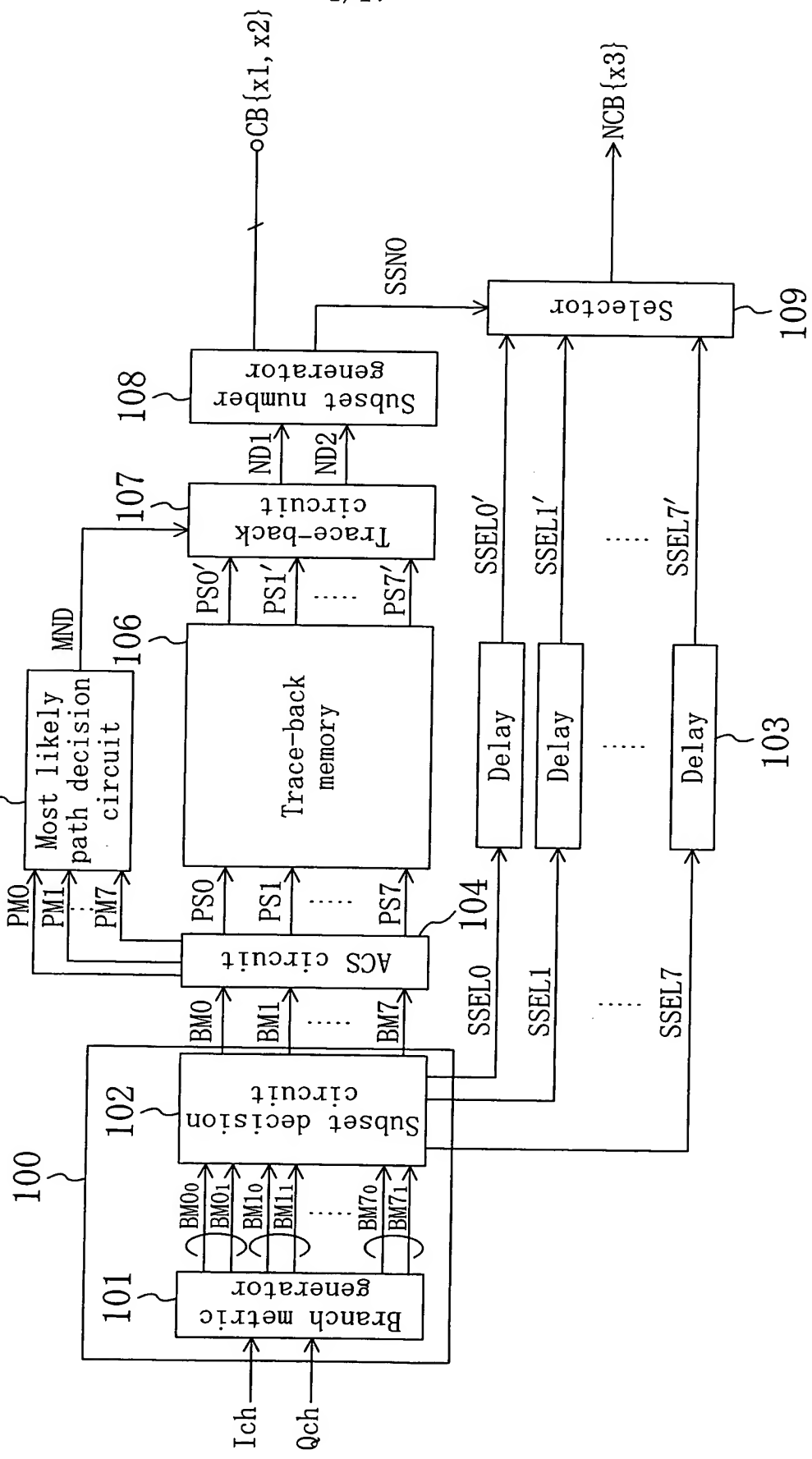

Ich
Qch
100
Branch metric generator
101
Subset decision circuit
102
ACS circuit
104
Most likely path decision circuit
105
Trace-back memory
106
Trace-back circuit
107
Subset number generator
108
Selector
109
Delay
103
BM0
BM1
BM7
BM0₀
BM0₁
BM1₀
BM1₁
BM7₀
BM7₁
PM0
PM1
PM7
PS0
PS1
PS7
PS0′
PS1′
PS7′
MND
ND1
ND2
SSN0
SSEL0
SSEL1
SSEL7
SSEL0′
SSEL1′
SSEL7′
CB{x1, x2}
NCB{x3}

Fig. 2

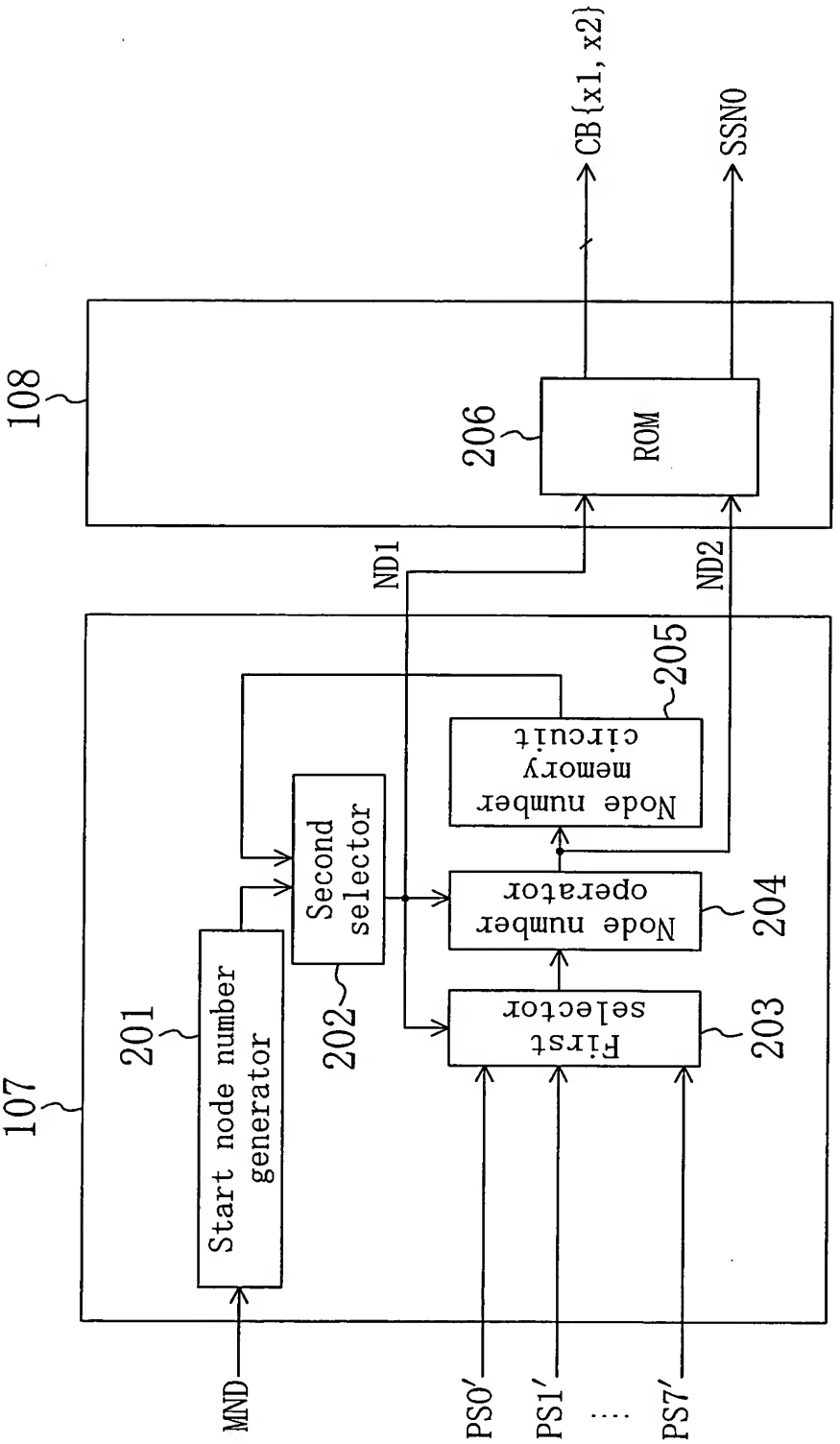

CB{x1, x2}
SSN0
108
206
ROM
ND1
ND2
205
Node number memory circuit
Second selector
202
Node number operator
204
First selector
203
201
Start node number generator
107
MND
PS0′
PS1′
....
PS7′

Fig. 3

ND2 \ ND1	000	001	010	011	100	101	110	111
000	00/0	10/4	01/2	11/6				
001					00/1	10/5	01/3	11/7
010	10/4	00/0	11/6	01/2				
011					10/5	00/1	11/7	01/3
100	01/2	11/6	00/0	10/4				
101					01/3	11/7	00/1	10/5
110	11/6	01/2	10/4	00/0				
111					11/7	01/3	10/5	00/1

CB{x2, x1}/SSNO

Fig. 4

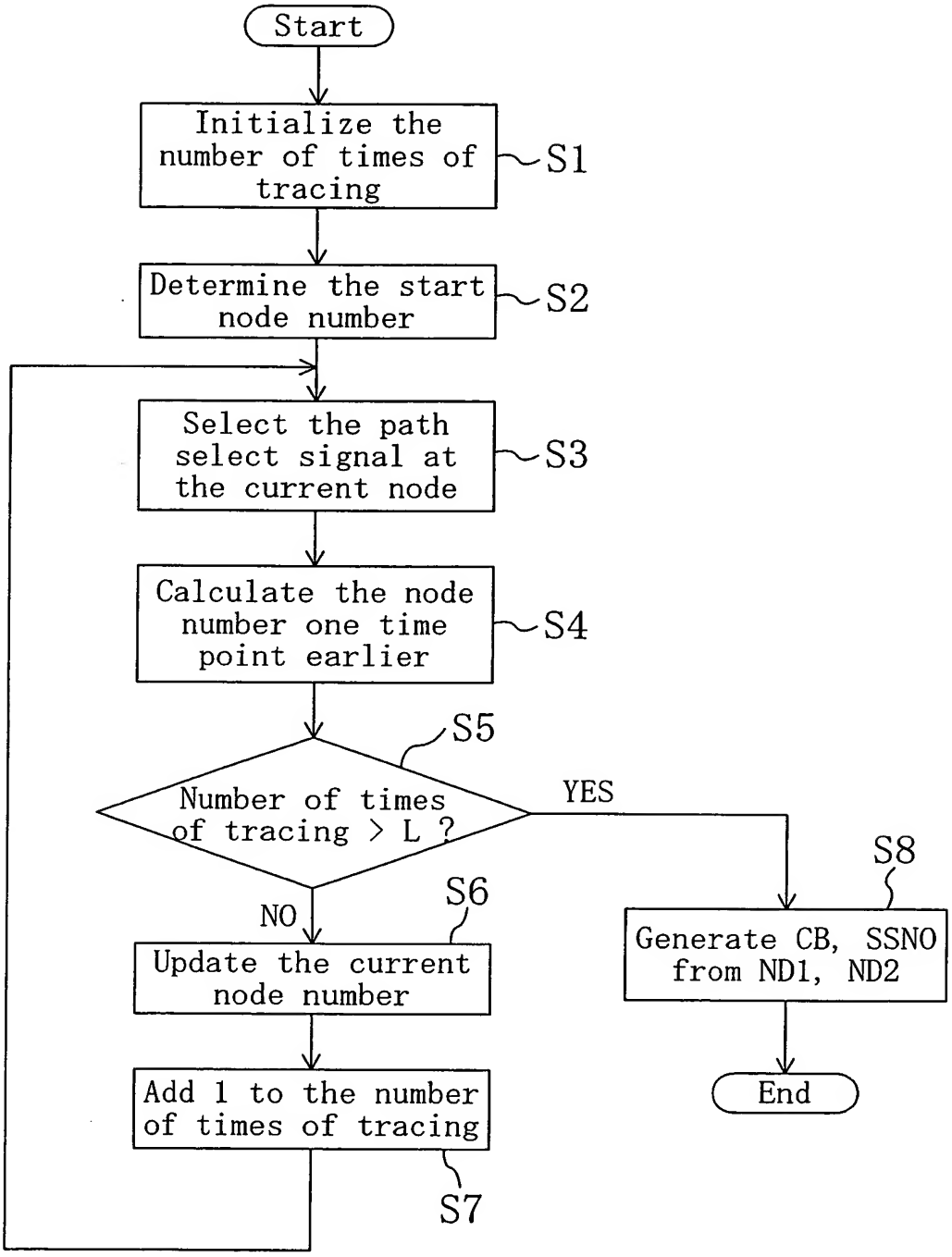

Start
Initialize the number of times of tracing
S1
Determine the start node number
S2
Select the path select signal at the current node
S3
Calculate the node number one time point earlier
S4
S5
Number of times of tracing > L ?
YES
NO
S6
Update the current node number
Add 1 to the number of times of tracing
S7
S8
Generate CB, SSNO from ND1, ND2
End

Fig. 5

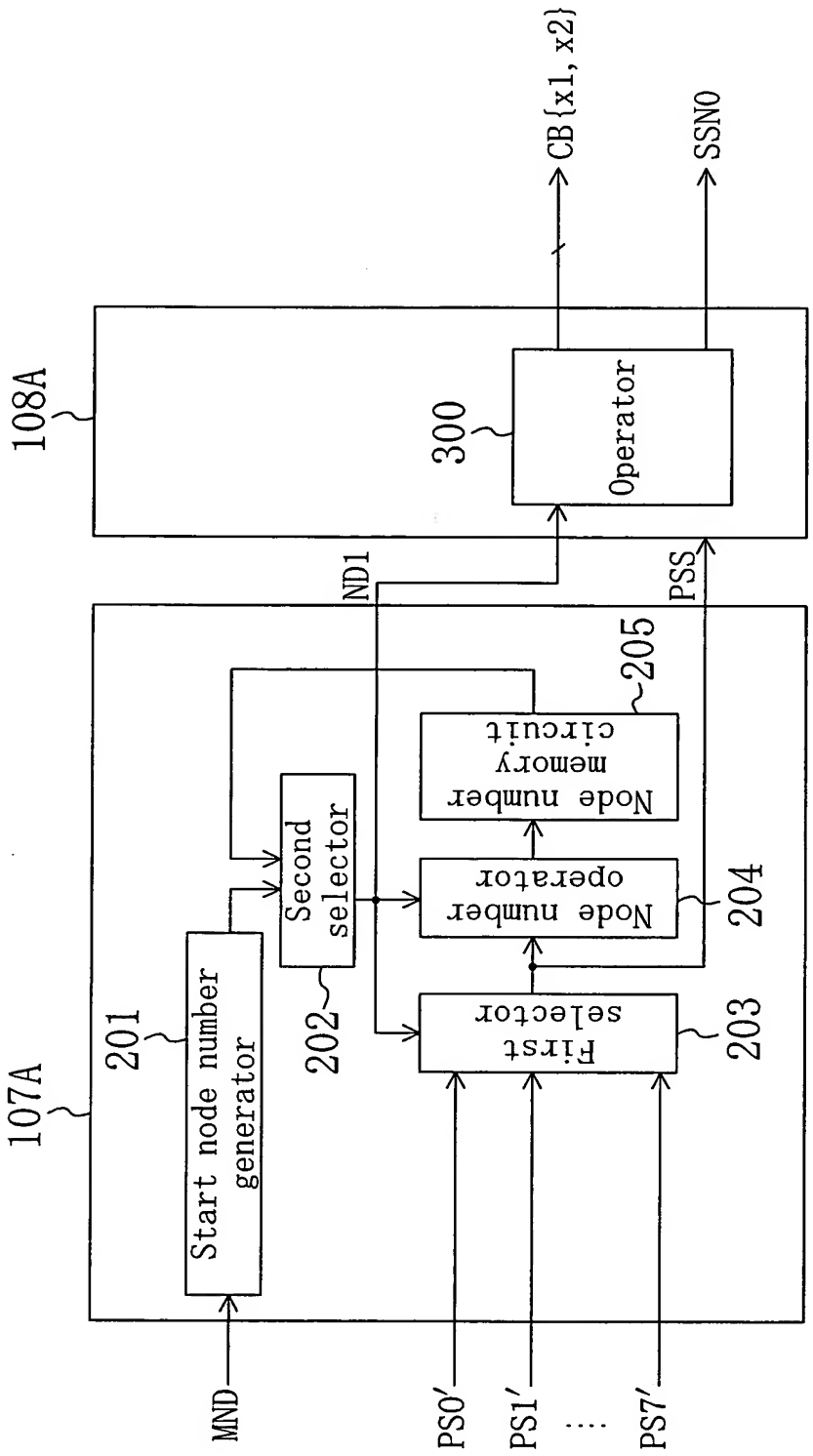

CB{x1, x2}
SSN0
108A
300
Operator
ND1
PSS
205
Node number memory circuit
Second selector
Node number operator
204
First selector
203
202
201
Start node number generator
107A
MND
PS0′
PS1′
....
PS7′

Fig. 6

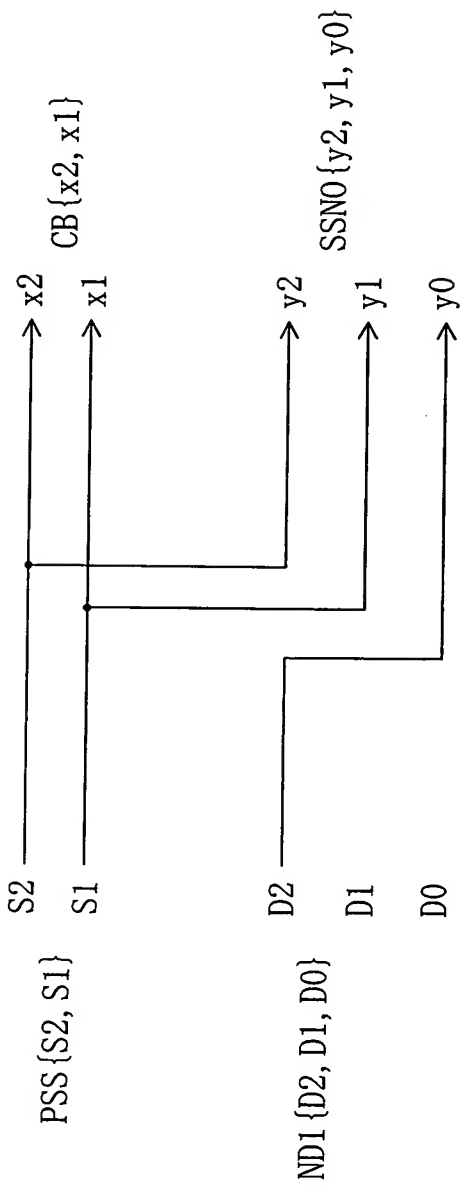

S2
S1
D2
D1
D0
PSS{S2, S1}
ND1{D2, D1, D0}
x2
x1
y2
y1
y0
CB{x2, x1}
SSNO{y2, y1, y0}

Fig. 7
Prior Art

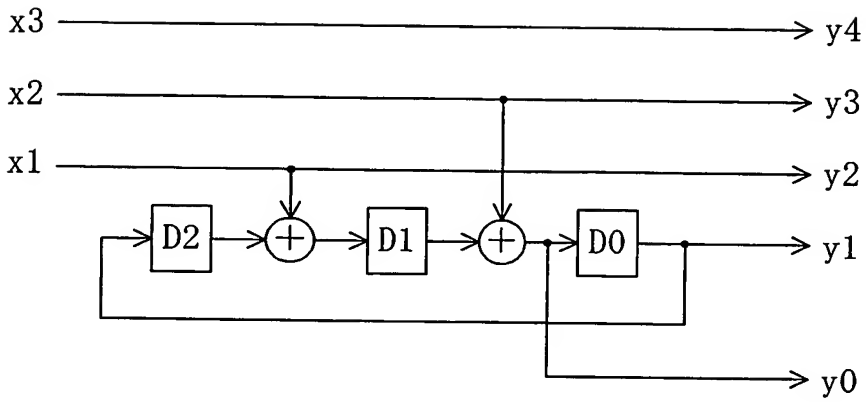


Fig. 8

Prior Art

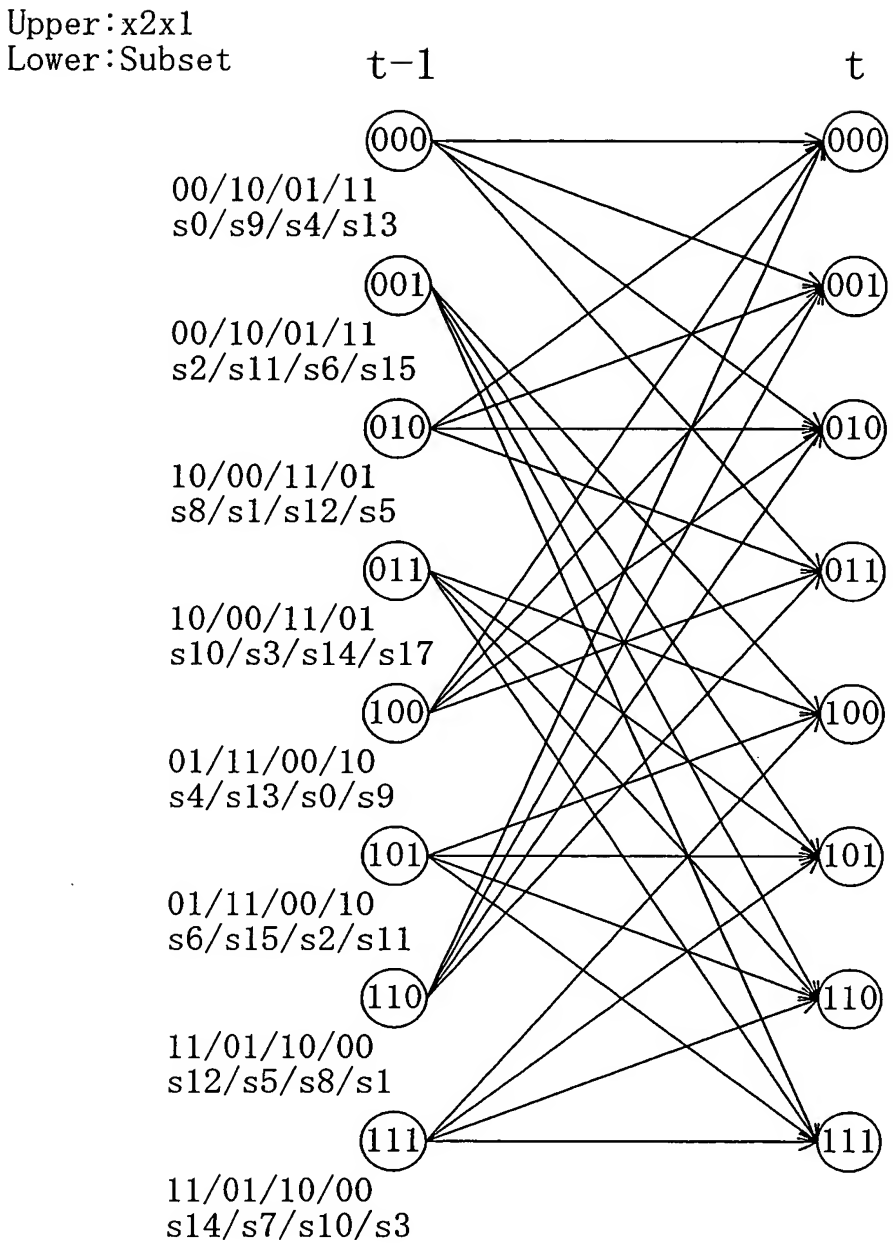


Fig. 9

ND2 \ ND1	000	001	010	011	100	101	110	111
000	00/0	10/9	01/4	11/13				
001					00/2	10/11	01/6	11/15
010	10/8	00/1	11/12	01/5				
011					10/10	00/3	11/14	01/7
100	01/4	11/13	00/0	10/9				
101					01/6	11/15	00/2	10/11
110	11/12	01/5	10/8	00/1				
111					11/14	01/7	10/10	00/3

CB{x2, x1}/SSN0

Fig. 10

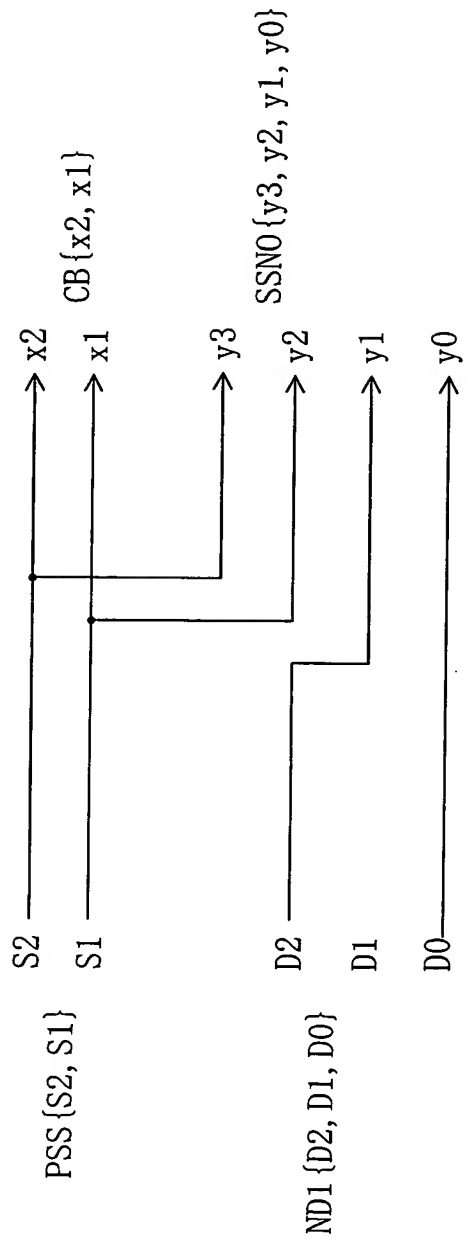

PSS{S2, S1}
S2
S1
CB{x2, x1}
x2
x1
ND1{D2, D1, D0}
D2
D1
D0
SSNO{y3, y2, y1, y0}
y3
y2
y1
y0

Fig. 11
Prior Art

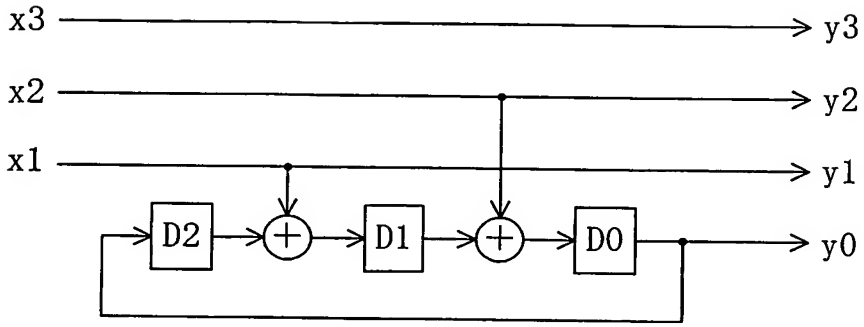


Fig. 12
Prior Art

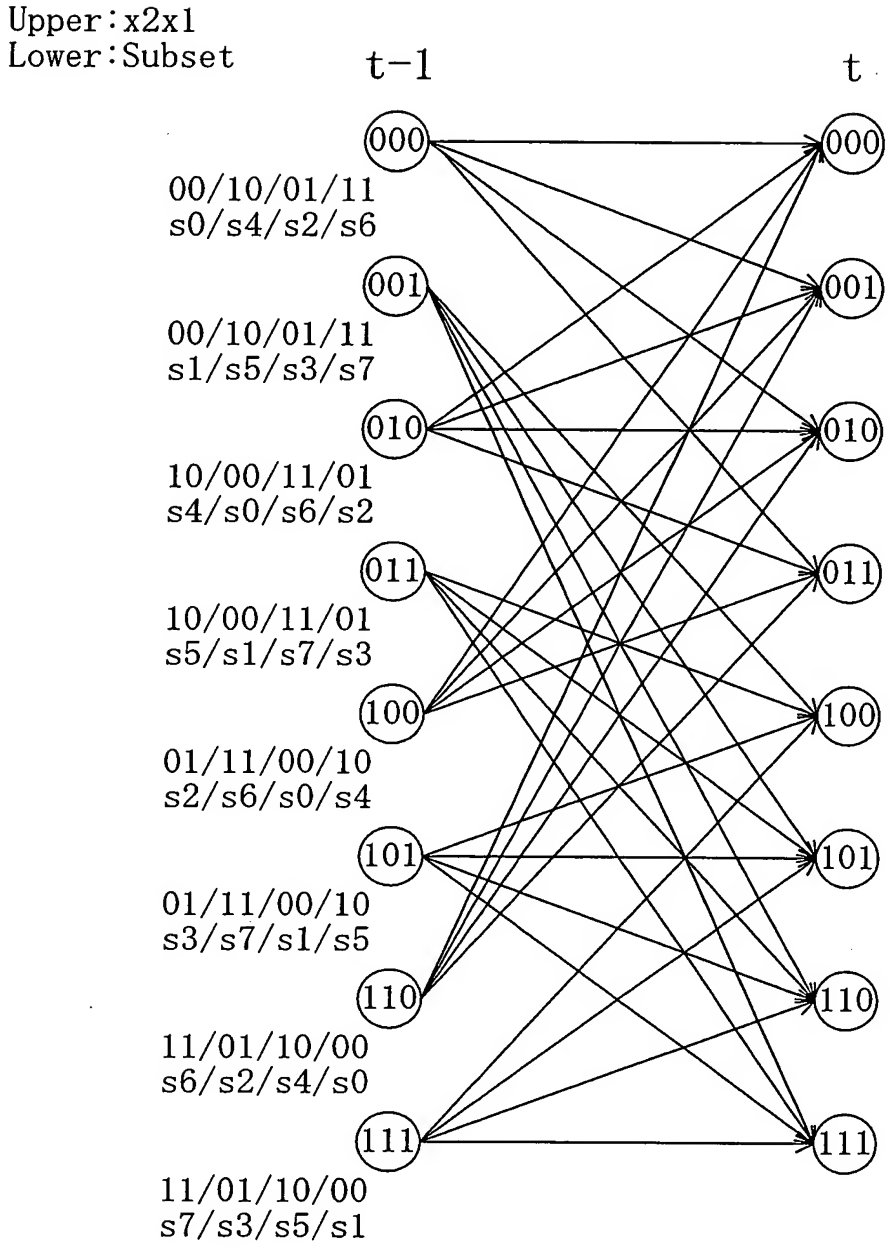


Fig. 13
Prior Art

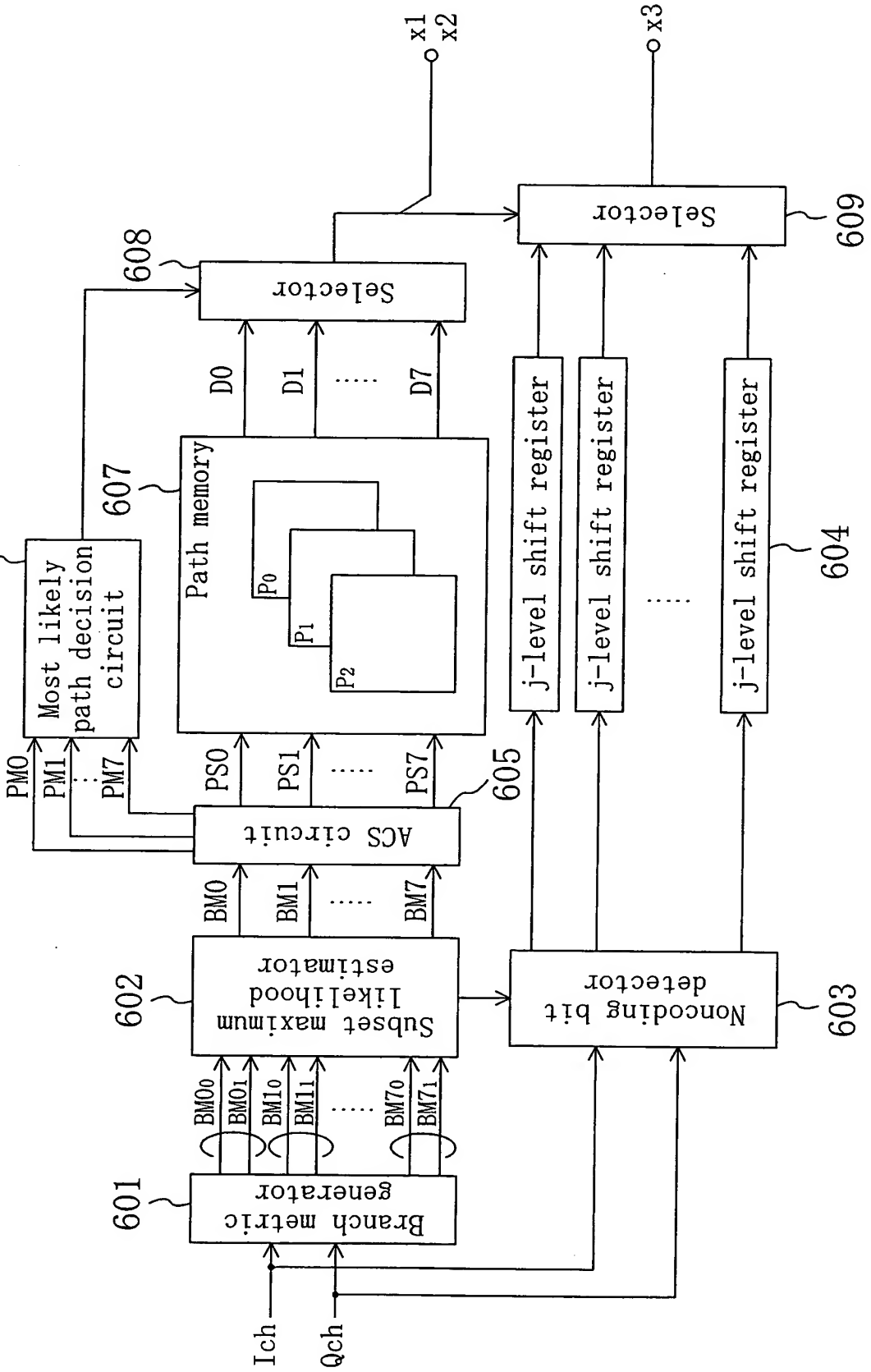


Fig. 14
Prior Art

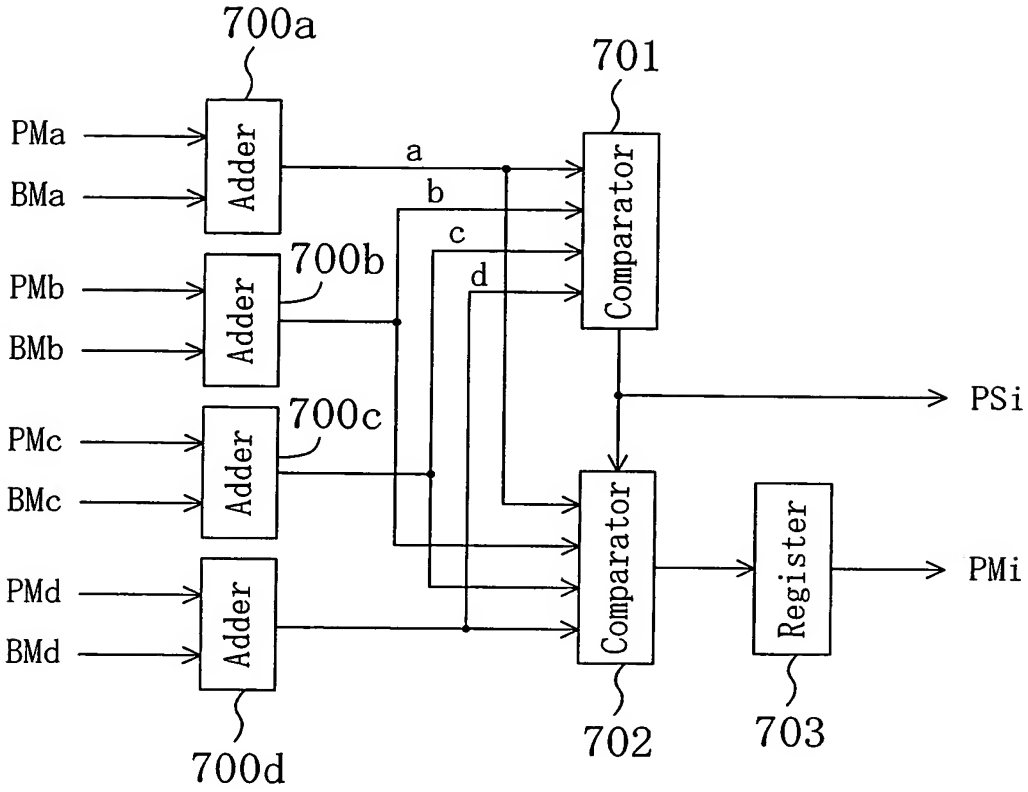


Fig. 15
Prior Art

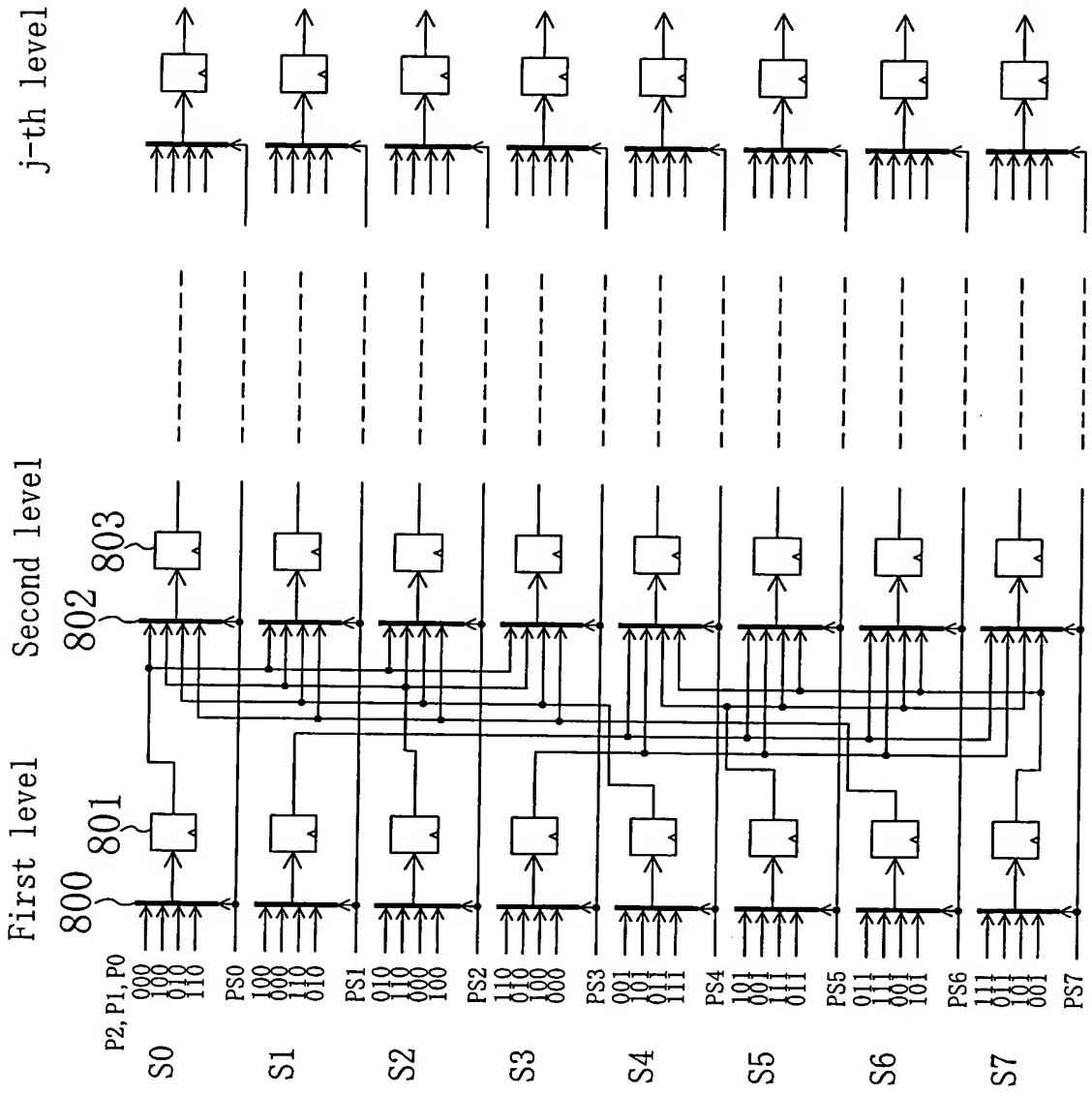
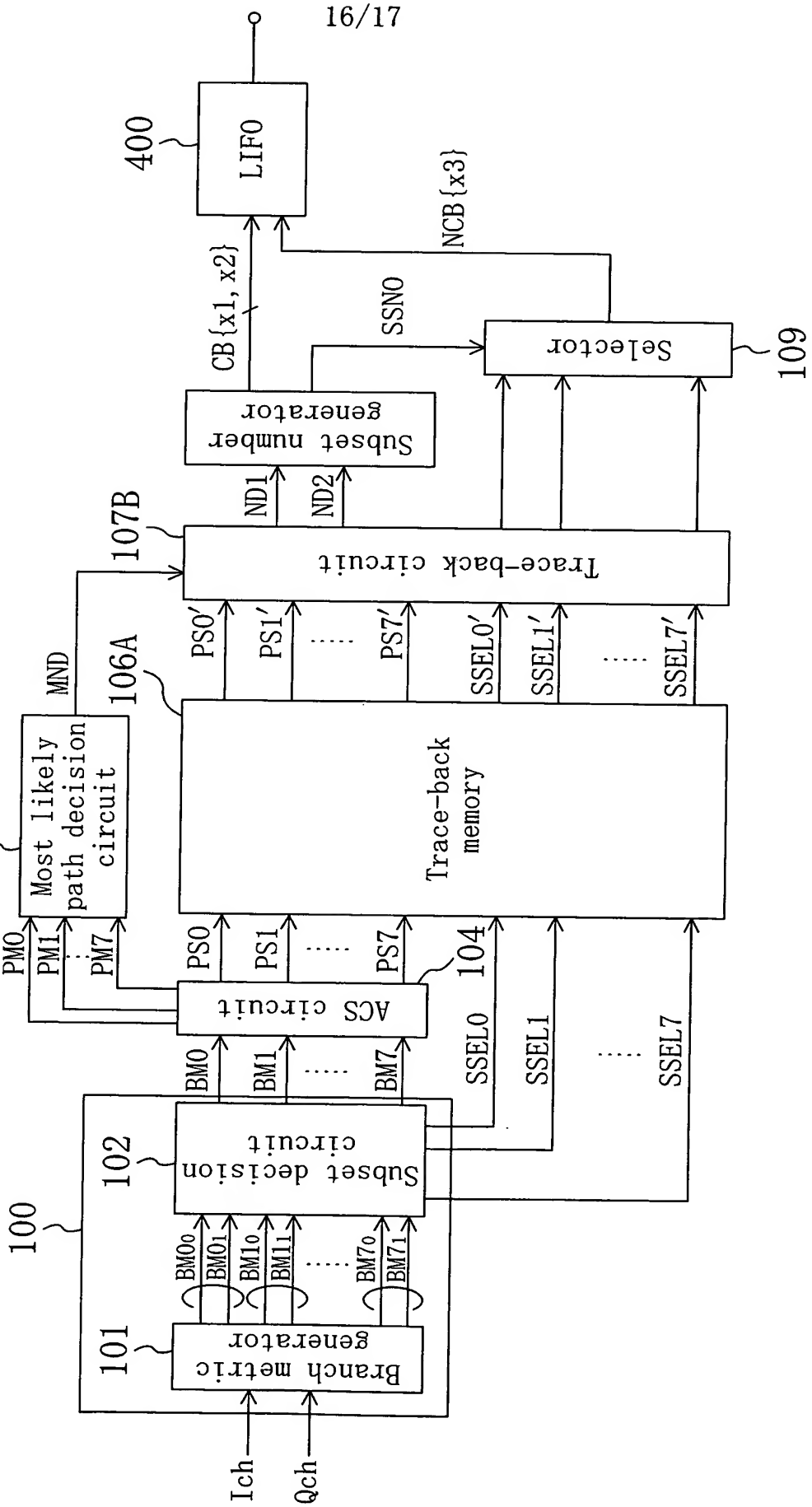


Fig. 16


Ich
Qch
100
Branch metric generator
101
Subset decision circuit
102
BM0
BM1
BM7
ACS circuit
104
PM0
PM1
PM7
PS0
PS1
PS7
Most likely path decision circuit
105
MND
Trace-back memory
106A
PS0′
PS1′
PS7′
SSEL0
SSEL1
SSEL7
SSEL0′
SSEL1′
SSEL7′
Trace-back circuit
107B
ND1
ND2
Subset number generator
CB{x1, x2}
SSN0
Selector
109
NCB{x3}
LIF0
400

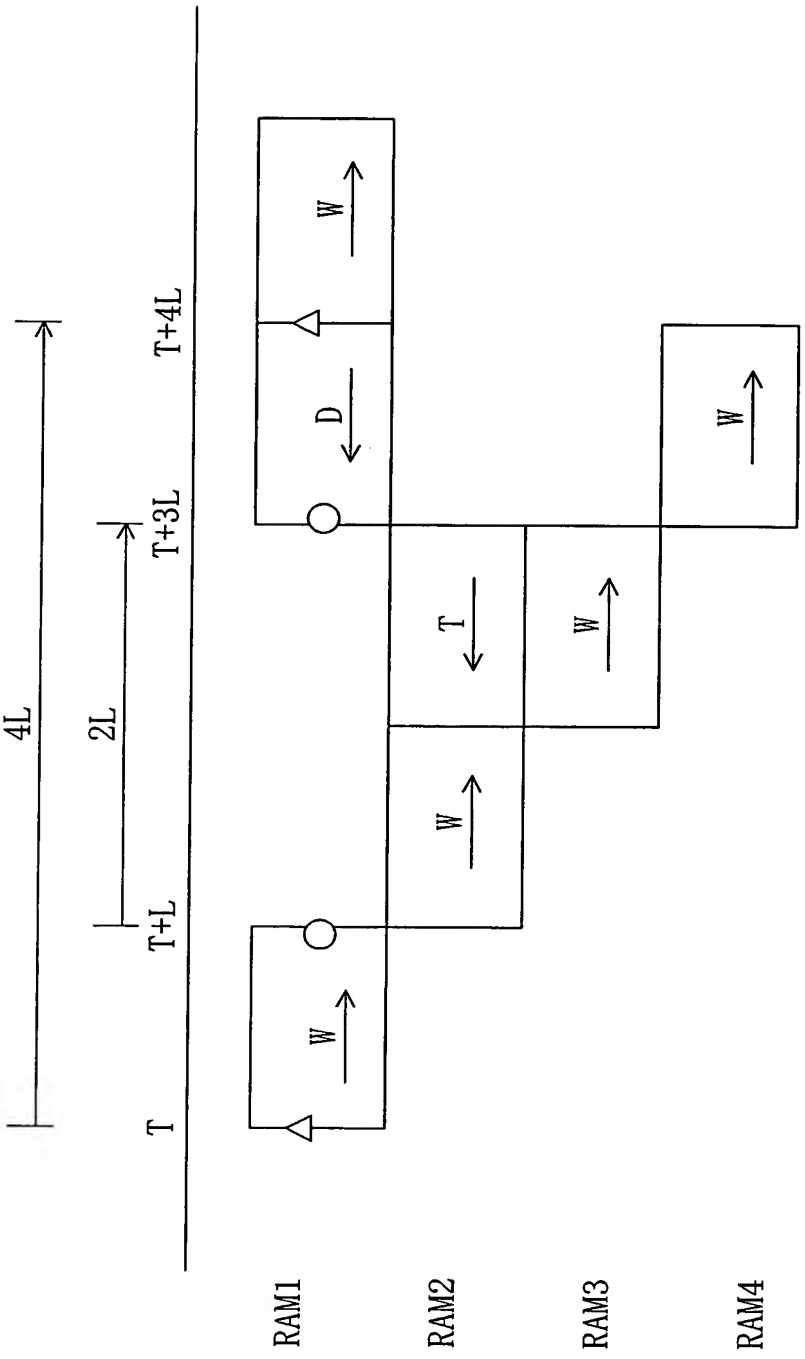



Fig. 17